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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:  
YIN TAT MA

Examiner: D.H. Patel

Group Art Unit: 2836

SERIAL NO. : 10/501,651

FILED: JAN. 10, 2005

FOR: ON-CHIP ESD PROTECTION  
CIRCUIT FOR COMPOUND  
SEMICONDUCTOR  
HETEROJUNCTION BIPOLAR  
TRANSISTOR RF CIRCUITS

**AMENDMENT AFTER FINAL**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In reply to the final Office Action mailed Feb. 2, 2007, please enter the following amendments and consider the following remarks.

A check for additional claim fees is included. The Office is also authorized to charge all fees under 37 CFR § 1.17, or all required extension of time fees or any deficit and credit any surplus in such fees to our deposit account #01-1960.

**Amendments to the Claims** begin on page 2.

**Remarks** begin on page 9.